ISSUE CLASSIFICATION

Class	Subclass

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PATENT NUMBER

U.S. UTILITY Patent Application

O.I.P.E.

SCANNED 15 Q.A. CR

PATENT DATE

APPLICATION NO.	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
09/925080	D F	438	515	~~2812~~ 2825	Luu

APPLICANTS: Ferruccio Frisina

TITLE: Method of manufacturing an integrated edge structure for high voltage semiconductor devices, and related integrated edge structure

PTO-2040 12/99

ISSUING CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)	
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)

INTERNATIONAL CLASSIFICATION

☐ Continued on Issue Slip Inside File Jacket

TERMINAL DISCLAIMER

☐ The term of this patent subsequent to ______ (date) has been disclaimed.

☐ The term of this patent shall not extend beyond the expiration date of U.S Patent. No. ______

☐ The terminal ____ months of this patent have been disclaimed.

DRAWINGS

Sheets Drwg.	Figs. Drwg.	Print Fig.

(Assistant Examiner) (Date)

(Primary Examiner) (Date)

(Legal Instruments Examiner) (Date)

CLAIMS ALLOWED

Total Claims	Print Claim for O.G.

NOTICE OF ALLOWANCE MAILED

ISSUE FEE

Amount Due	Date Paid

ISSUE BATCH NUMBER

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